

X4 - Errata

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1. IC Anomalies

This section lists the anomalies found in the different revisions of the X4 IC.

ID	Module	Description	Affects revision
001	Timing	PLL may in rare cases fail to lock.	1,2

Table 1.1. IC Anomalies Overview

1.1. [001] - PLL may in rare cases fail to start

The VCO in the RX and TX PLLs on the device may in very rare cases fail to start oscillating when the PLL is powered on. The problem is caused by the ring VCO entering a non-oscillating steady state. Once the VCO has entered the non-oscillating state, the entire PLL needs to be powered down before it can be re-started, as it is unable to exit the failed state on its own.

Leaving the PLL in the non-oscillating state may accelerate the degradation of the gates in the VCO, due to high current density in the ring oscillator. Remaining in this state for an extended amount of time may cause permanent damage.

1.1.1. Symptoms

The PLL lock signal is never asserted after starting the PLL. This is manifested in SW by the functions x4driver_setup_default() and x4driver_init() returning XEP_ERROR_X4DRIVER_COMMON_PLL_LOCK.

1.1.2. Conditions

The likelihood of entering the non-oscillating state increases with higher supply voltage.

A device in the non-oscillating state may be damaged quicker at higher supply voltages.

1.1.3. Workaround

Do not power on the RX and TX PLLs by writing directly to the PLL control register over SPI. Instead, use the new PLL startup procedure implemented in version 11 of the X4 firmware. The new version of the x4driver software, provided by Novelda, includes the updated X4 firmware, and is using the recommended PLL startup procedure.

The recommended PLL startup procedure detects if the PLL does not lock within the expected time and then powers down the PLL, waits for a predefined amount of time to allow oscillations and voltages to drop, and then attempt to start the PLL again. Multiple startup attempts are done with a varying delay between power-down and startup.

In addition to the firmware workaround, the supply voltage should be limited to 1.8 V.



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Document History

Rev.	Release date	Change description
Α	01-July-2021	First release